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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/893,791	06/29/2001	Yutaka Kobayashi	PNDF-01068	4575

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/893,791	KOBAYASHI, YUTAKA	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 4 and 16 - 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 4 and 16 - 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's amendment filed on December 30, 2002 has been received and entered in the case.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Song et al.

Regarding claim 1, the acknowledged prior art discloses in Fig. 1 a semiconductor device, comprising:

- a semiconductor chip (100);
- a chip-mounting substrate (103) which is provided with the semiconductor chip mounted on a top surface thereof and first conductive pads (107) formed on a bottom surface thereof and connected with the semiconductor chip electrically;
- solder balls (106) formed on the first conductive pads;
- a printed circuit board (104) on which second conductive pads (108) connected with the solder balls are formed; and
- underfill material (105) injected into a clearance formed between the chip-mounting substrate and the printed circuit board,

The acknowledged prior art does not disclose uneven roughness being formed on a surface, uneven roughness existing a bottom surface of the chip-mounting substrate and the uneven roughness on said bottom surface increasing an area of a contact surface. Song et al. discloses in Fig. 3 and column 3, line 61 ~ column 4, line 4 uneven roughness (30) being formed on a surface (10b) which is brought into contact with a material (90) of at least one of a chip-mounting substrate (10), the uneven roughness (30) existing a bottom surface (10b) of the chip-mounting substrate (10) and the uneven roughness (30) on said bottom surface increasing an area of a contact surface between the chip-mounting substrate and the underfill material. It would have been obvious to one of ordinary skill in the art at the time of the present invention was made to use the uneven rough surface of Song et al. in the device of the acknowledged prior art

of Fig. 1 in order to enhance the bonding strength as taught by Song et al. in column 3, lines 67 ~ column 4, line 1.

Regarding claim 3, Song et al. discloses in Fig. 3 and column 3, line 61 the uneven roughness being shaped into at least one of a slit-like configuration and a dimple-like configuration.

4. Claims 2 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Song et al. as applied to claim 1 above, and further in view of Enomoto et al.

Regarding claim 2, The acknowledged prior art of Fig. 1 and Song et al. disclose a claimed invention except for the uneven roughness being formed on at least one of the first conductive pads and the second conductive pads selectively. However, Enomoto et al. discloses in Fig. 1d an uneven roughness being formed on an second conductive pads (6). It would have been obvious to one of ordinary skill in the art at the time of the present invention was made to use the uneven roughness of Enomoto et al. in the device of the acknowledged prior art of Fig. 1 and Song et al. in order to provide an adhesive for the printed circuit board having excellent thermal resistance, electrical resistance, chemical stability and adhesion property to the printed circuit board as taught by Enomoto et al. in column 2, lines 43 ~ 48.

Regarding claim 16, Enomoto et al. discloses in Fig. 1d the printed circuit board having a dimple-like shaped configuration.

5. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Song et al. as applied to claim 1 above, and further in view of Kaskoun et al.

The acknowledged prior art of Fig. 1 and Song et al. disclose a claimed invention except for a surface of said chip-mounting substrate having a slit-like shaped configuration. However, Kaskoun et al. discloses in Fig. 1 a surface of said chip-mounting substrate (13) having a slit-like shaped configuration. It would have been obvious to one of ordinary skill in the art at the time of the present invention was made to use the slit-like shaped configuration of Kaskoun et al. in the device of the acknowledged prior art of Fig. 1 and Song et al. in order to decrease tacking pressure during the assembly process as taught by Kaskoun et al. in column 3, lines 62 ~ 63.

6. Claims 4, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kweon et al. in view of Sato et al.

Kweon et al. discloses in Fig. 2A a semiconductor device, comprising:

- a semiconductor chip (21);
- a lead frame (23, 25 and 27) which is provided with the semiconductor chip mounted thereon and electrically connected with the semiconductor chip; and
- a printed circuit board (28) including third conductive pads (29), which are formed thereon and brought into direct contact with the lead frame.

Kweon et al. does not disclose at least one of the lead frame and the printed circuit board being provided with uneven rough contact surfaces in direct contact therebetween and the uneven roughness exists on a bottom surface of the lead frame. Sato et al. discloses in Fig. 7A,

Fig. 14C and Fig. 16A at least one of a lead frame (27 in Fig. 7A) and a printed circuit board (48) being provided with uneven rough contact surfaces (16a in Figs. 14C and 16A) in direct contact therebetween and the uneven roughness (16-1 in Fig. 16A) exists on a bottom surface of the lead frame. It would have been obvious to one of ordinary skill in the art at the time of the present invention was made to use the uneven rough contact surfaces of Sato et al. in the device of Kweon et al. in order to increase the strength of the external terminal as taught by Sato et al. in column 10, lines 41 ~ 43.

Regarding claim 18, Sato et al. discloses in Fig. 7A, Fig. 14C and Fig. 16A lead frame (27) comprising a lead (14), said lead comprising an inner lead portion (14a) connected to an outer lead portion (16), said outer lead portion comprising the uneven roughness (16-1 in Fig. 16A).

Regarding claim 19, Sato et al. discloses in Fig. 7A, Fig. 14C and Fig. 16A the uneven roughness (16-1) existing on contact surfaces (16a) between a pad (52) of said printed circuit board (48) and an outer lead (16) of said lead frame (27).

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Lee.

The acknowledged prior art discloses in Fig. 1 a semiconductor device, comprising:

- a semiconductor chip (100);
- a chip-mounting substrate (103) which is provided with said semiconductor chip mounted on a top surface thereof and first conductive pads (107) formed on a bottom

surface thereof and connected with said semiconductor chip electrically, said chip-mounting substrate including wirings (102);

- solder balls (106) formed on said first conductive pads;
- a printed circuit board (104) on which second conductive pads (108) connected with said solder balls are formed; and
- material injected (105) into a clearance formed between said chip-mounting substrate and said printed circuit board.

The acknowledged prior art does not disclose the wirings to be Cu and uneven roughness being formed on a contact surface between said Cu wirings of said chip-mounting substrate and said solder balls and the uneven roughness exists on a bottom surface of the Cu wirings, and said Cu wirings are connected to the solder balls to form a joined surface. Lee discloses in Fig. 5E and column 2, line 16 wirings to be Cu (100) and uneven roughness being formed on a contact surface between said Cu wirings (100) of a chip-mounting substrate (300) and solder balls (150). It would have been obvious to one of ordinary skill in the art at the time of the present invention was made to use the uneven rough contact surface of Lee in the device of the acknowledged prior art of Fig. 1 in order to increase a contact area as taught by Lee in column 3, lines 34 ~ 36.

Response to Arguments

8. Applicant's arguments with respect to claims 1 ~ 4, 18 and 20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yoshizawa et al. discloses an uneven surfaced Cu film.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
April 7, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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